Fig. 1

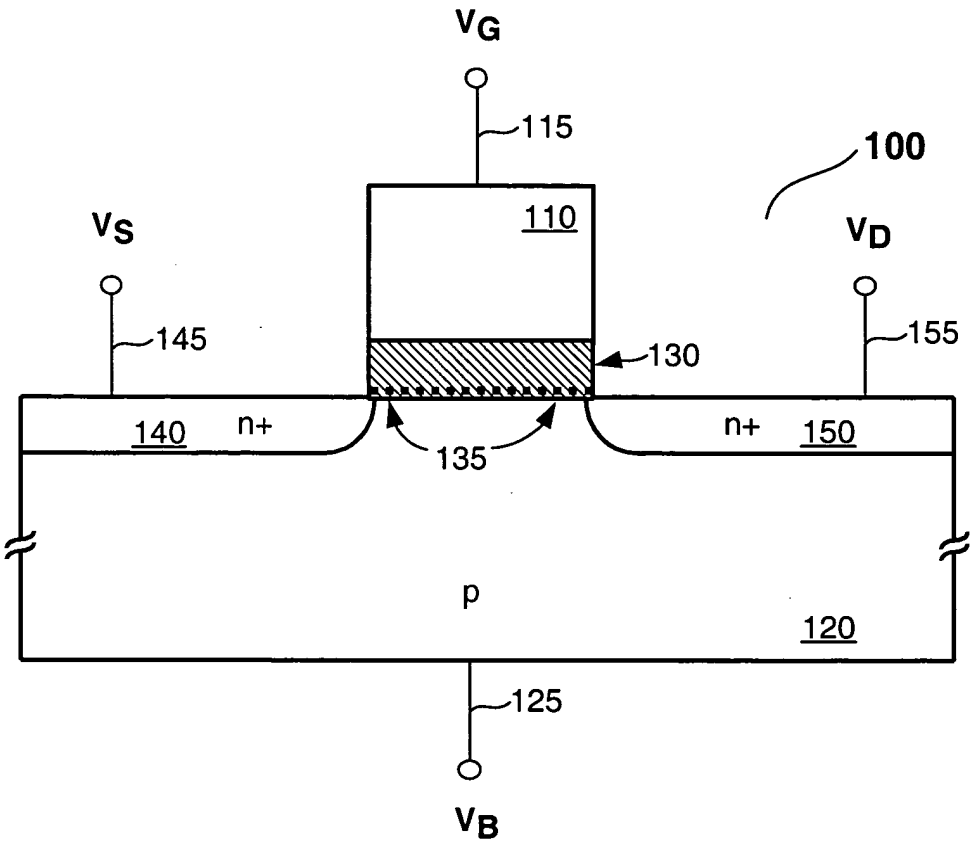

Fig. 2

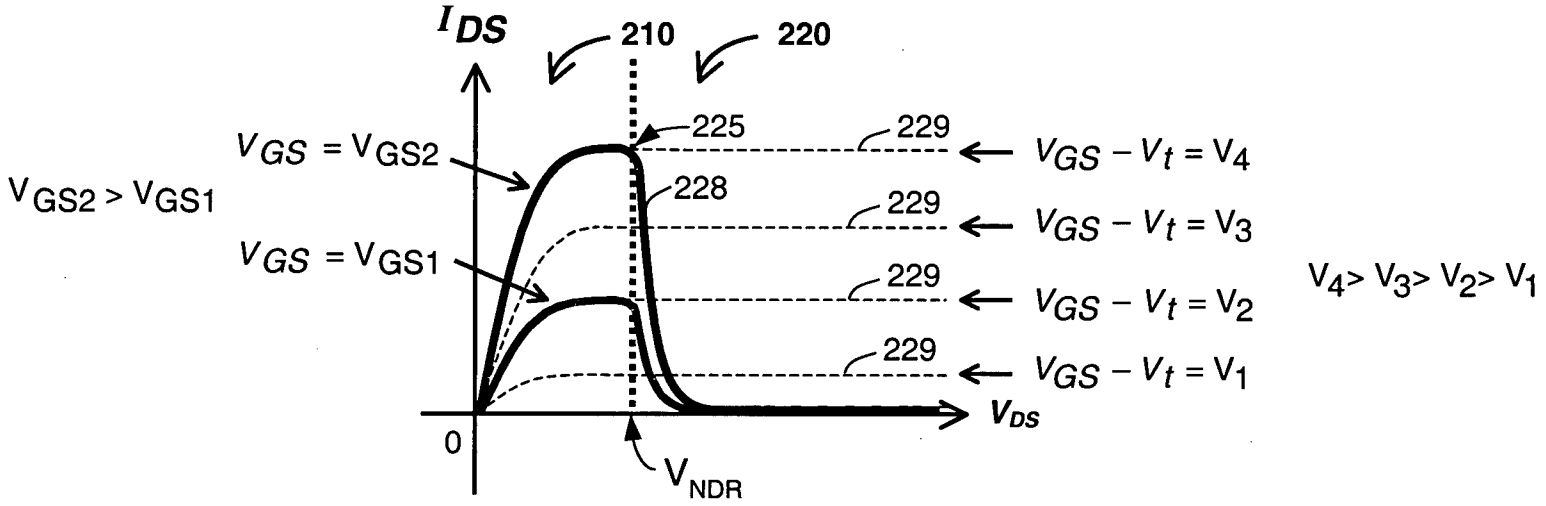
I_{DS}
210
220
225
229
228
V_{GS} = V_{GS2}
V_{GS} = V_{GS1}
V_{GS2} > V_{GS1}
$V_{GS} - V_t = V_4$
$V_{GS} - V_t = V_3$
$V_{GS} - V_t = V_2$
$V_{GS} - V_t = V_1$
$V_4 > V_3 > V_2 > V_1$
V_{DS}
0
V_{NDR}

Fig. 3

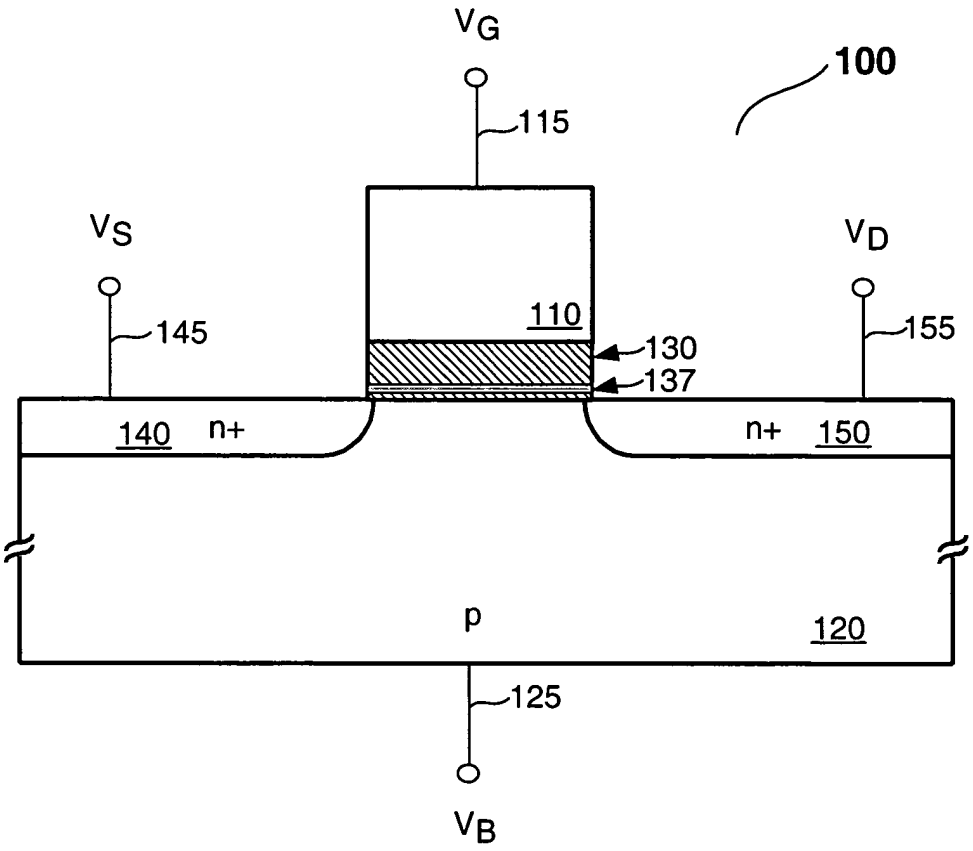

Fig. 4

Standard CMOS Starting Material
Standard CMOS Isolation Process
NDR Surface Doping Process Sequence
NDR Device Gate Insulator Formation
N-well Dopant Process Sequence (for PMOS)
P-well Dopant Process Sequence (For NMOS)
Logic Device Gate Oxidation
Gate Material Deposition and Patterning
NDR Drain Junction Engineering Sequence
Source/Drain Pattern and Process Sequence
Oxide Deposition
Contact Process Sequence
Metal Process Sequence